

Low-Resource Computing: The Resource-Adaptive Embedded Runtime (ALICE)

Operational Sovereignty for Contested,
Austere, and Long-Duration Environments

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Target: DARPA MX0/ST0 Phase I

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The von Neumann Illusion at the Extreme Edge

Laboratory Assumptions

Continuous 120V/240V Power Grid

Gigabytes of Pristine DDR SRAM

High-Bandwidth 5G/Wi-Fi

Sub-10nm Pristine Fabs

Tactical Realities

Intermittent Scavenging (**Nano-amps**)

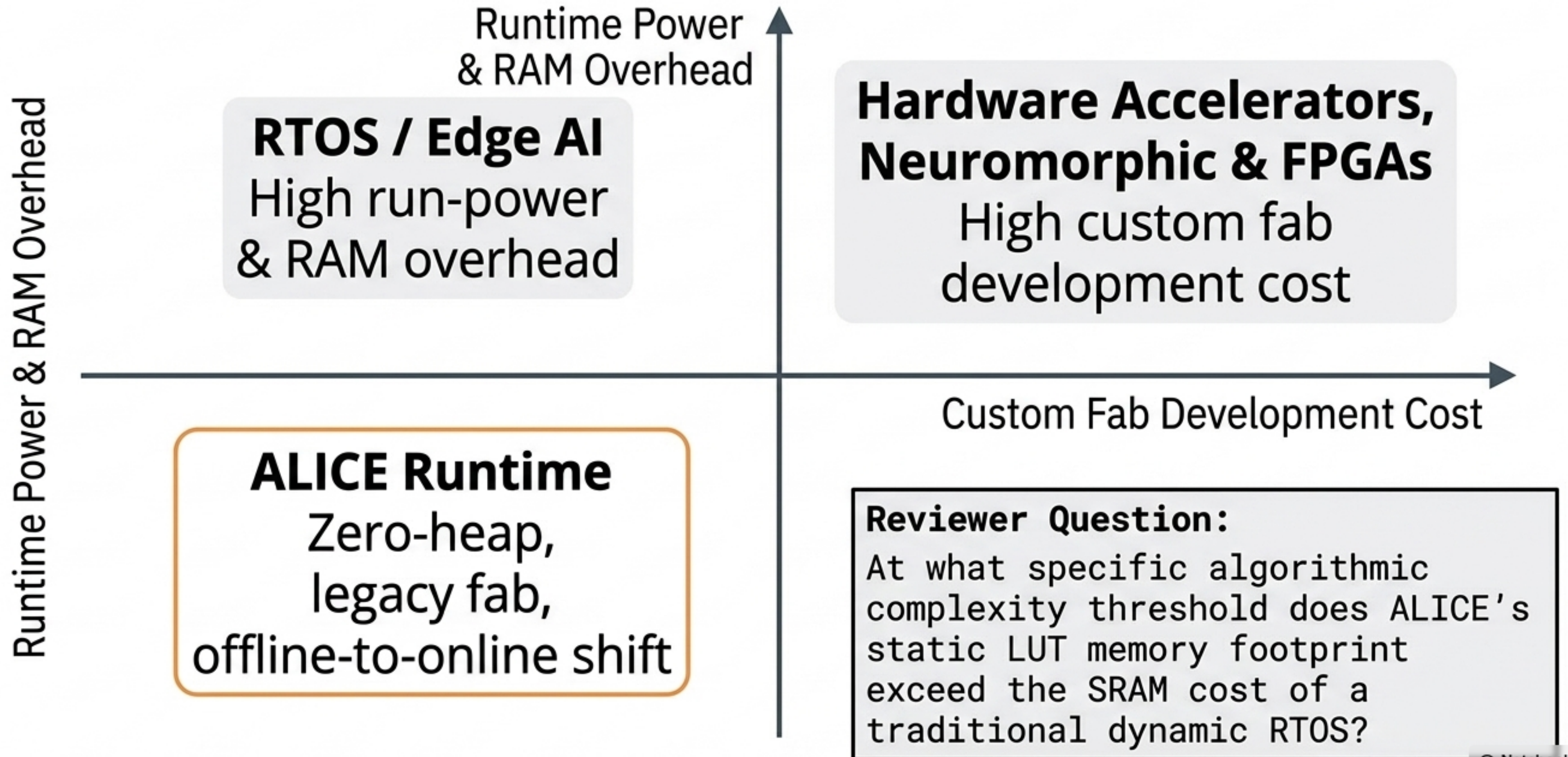
Severe Single-Event Upsets (SEUs)

Jammed/Denied RF Channels

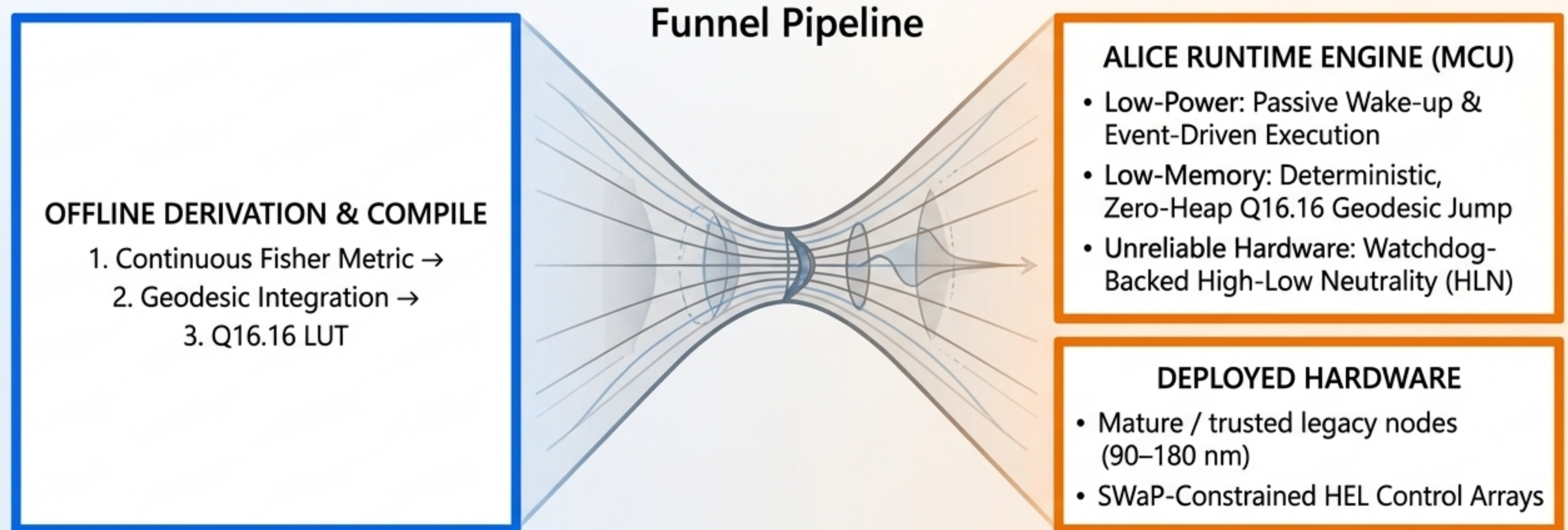
Reliance on **Coarse Legacy Silicon**

Modern embedded edge paradigms demand FPU, massive dynamic memory, and continuous active polling. When deployed in austere space or tactical environments, these prerequisites trigger catastrophic SWaP-C (Size, Weight, Power, and Cost) bottlenecks.

Navigating the Edge Computing Paradigm Spectrum

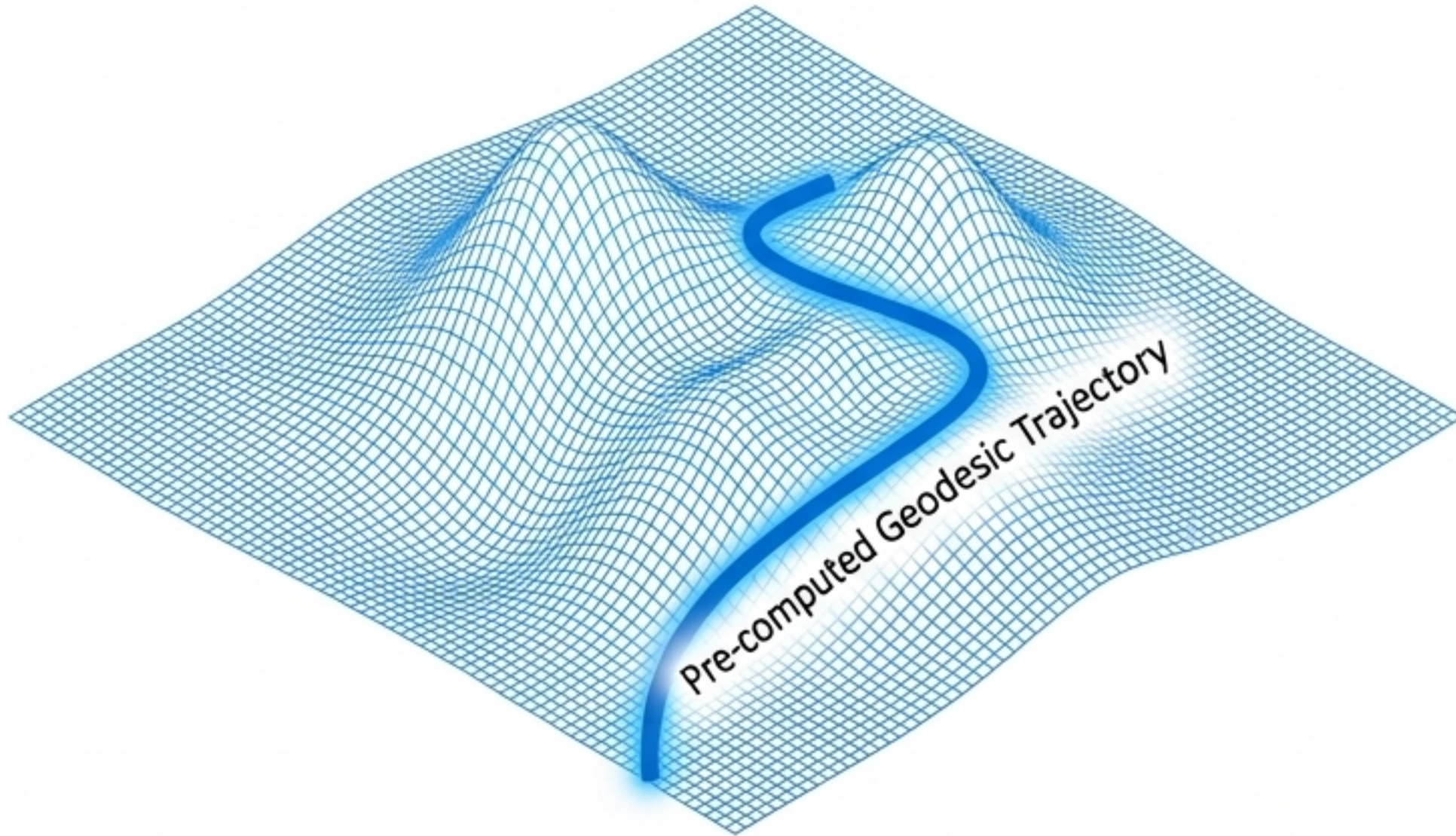


Shifting the Mathematical Burden: Offline-to-Online Computation



ALICE replaces continuous runtime numerical solvers with structural representations of state evolution. We compute the complex physics offline and deploy only the geometric coordinates online.

Mathematical Foundation: Navigating the Statistical Manifold



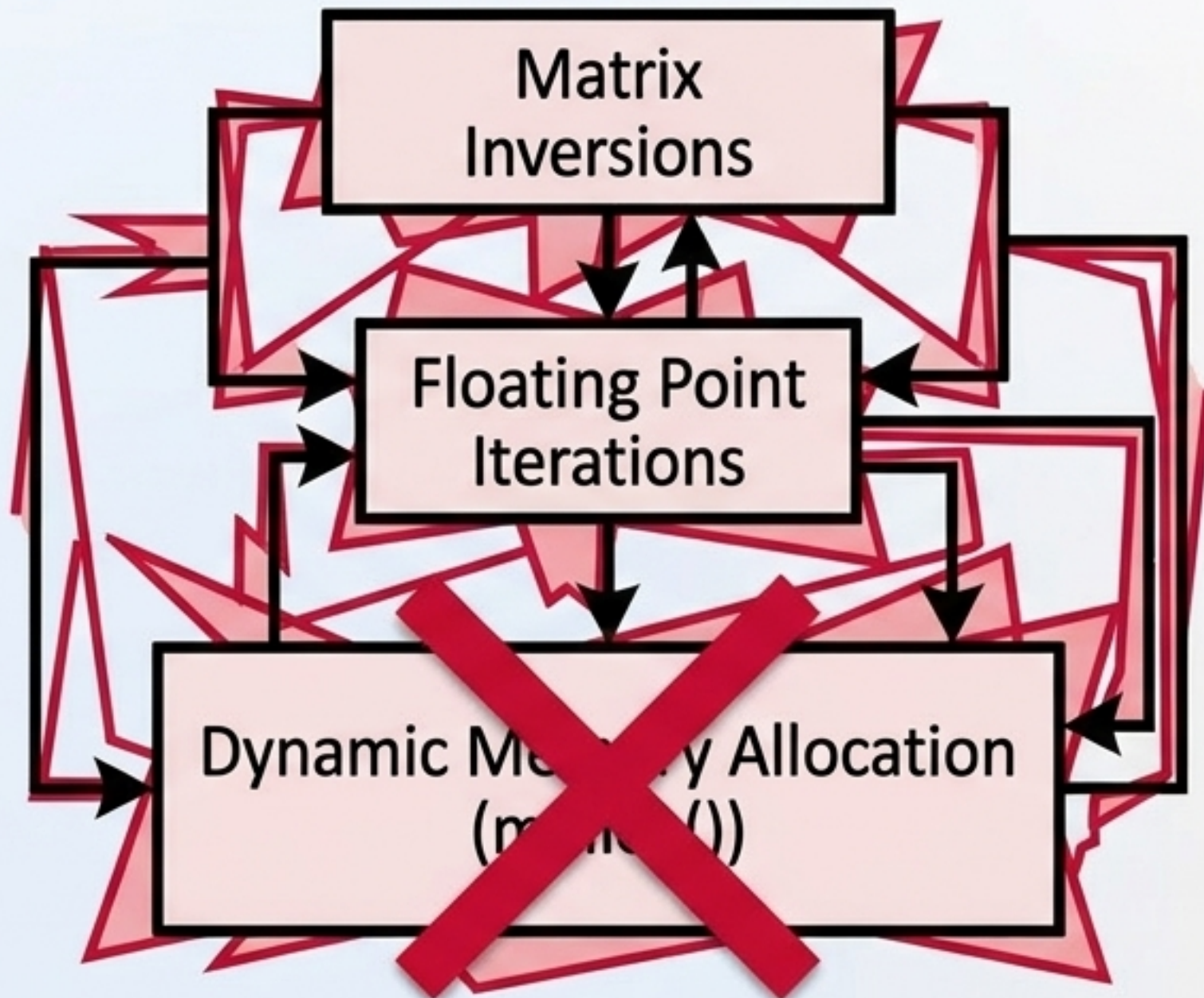
$$g_{\mu\nu}(\theta) = \frac{1}{2} \text{Tr} \left(\rho(\theta) \{ \hat{L}_\mu, \hat{L}_\nu \} \right)$$

- System states are mapped as coordinates on a continuous manifold governed by the QFIM.
- Christoffel symbols are computed offline to integrate geodesic trajectories.

Key Insight: The governing differential equations are entirely solved before the mission begins. The deployed node merely looks up its pre-calculated trajectory.

Fixed-Point Deterministic Execution: Eliminating the FPU

Traditional Solvers



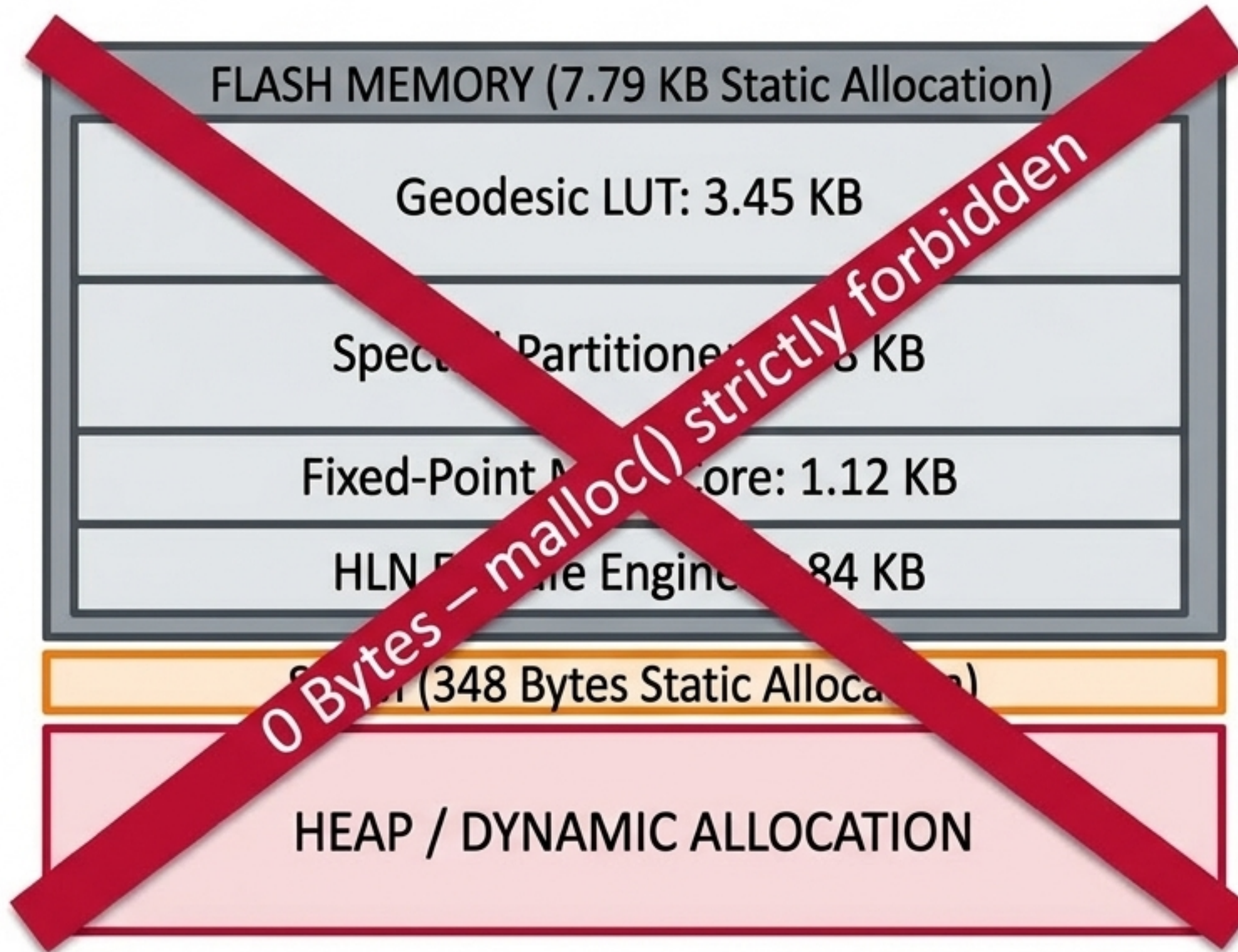
ALICE Pipeline

```
typedef int32_t fixed32_t;  
#define Q_FRAC_BITS 16  
#define Q_HALF      ((fixed32_t)(1 << (Q_FRAC_BITS - 1)))  
  
static inline fixed32_t q_mul(fixed32_t a, fixed32_t b) {  
    int64_t temp = (int64_t)a * (int64_t)b;  
    return (fixed32_t)((temp + Q_HALF) >> Q_FRAC_BITS);  
}
```

$$\theta_{\text{future}}^{\mu} = \theta_{\text{current}}^{\mu} + (\lambda \times \text{LUT}[\text{index}][\mu])$$

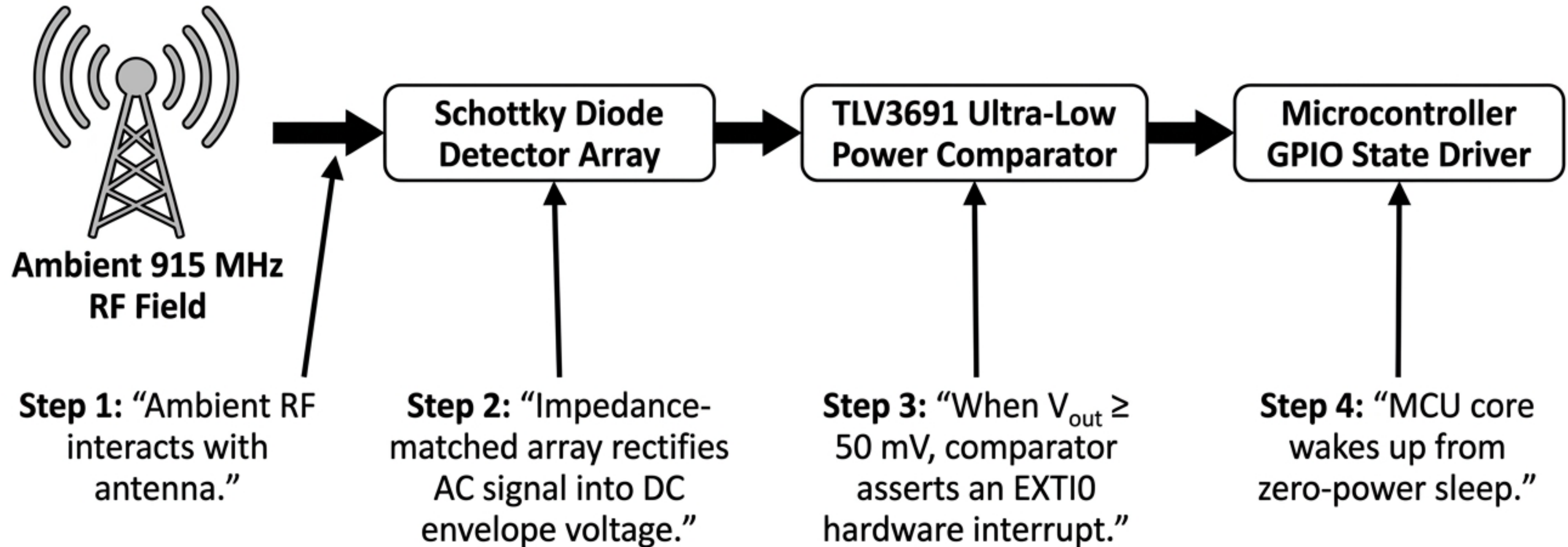
Reduces differential equation networks to microsecond bit-shifts and integer additions, ensuring strict bounded execution.

Memory Architecture: The Zero-Heap Mandate



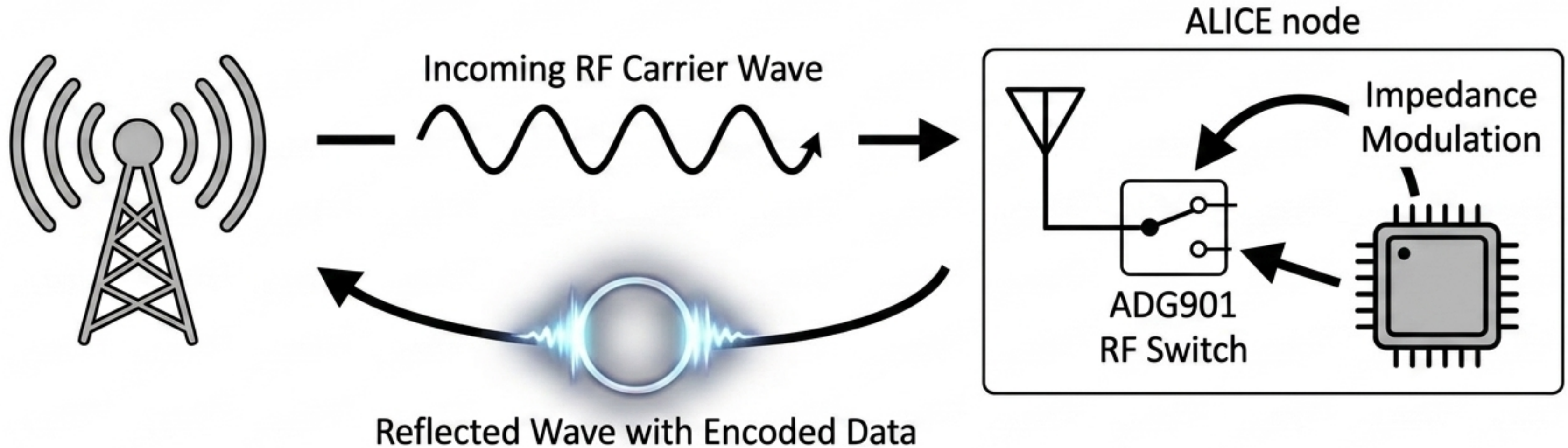
- ALICE completely forbids dynamic memory allocation.
- All required state spaces and geodesic jumps are statically pre-allocated.
- This eliminates memory fragmentation, prevents heap overflows, and guarantees deterministic processing latency on legacy logic gates.

Physics-First Computing: Passive RF Wake-up



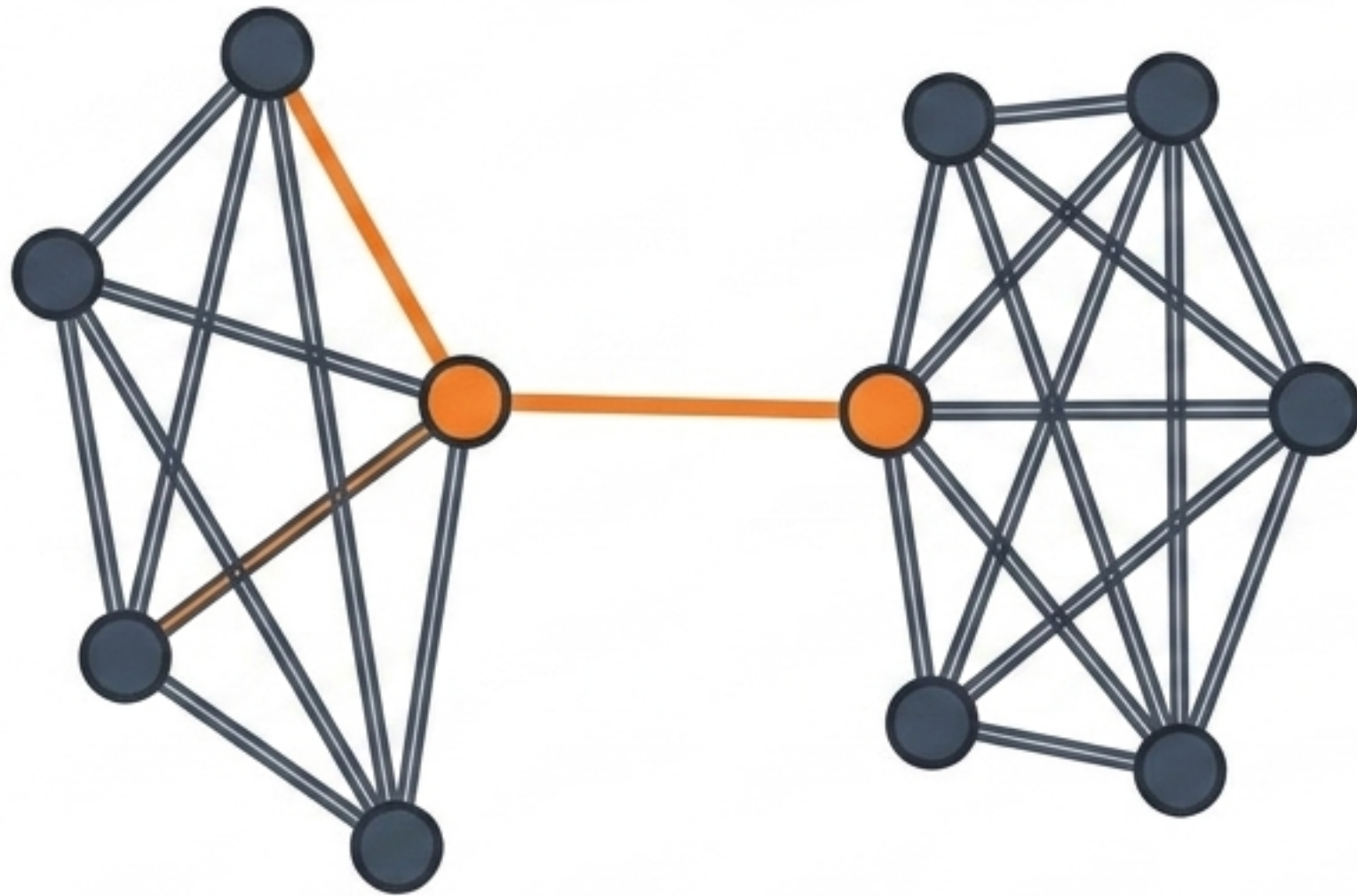
The node remains in a near-zero power sleep state, utilizing the macroscopic dipole moment of the material substrate to transduce ambient RF energy into a hard digital wake-up interrupt.

Telemetry via Passive Backscatter Modulation



ALICE abandons traditional power-hungry RF synthesizers and active transmitters. Telemetry is achieved **entirely** via **passive backscatter**. By toggling the impedance state of the antenna, the node **transmits diagnostic** of swirly signal, but transmits diagnostic geometry back to the source, remaining within a total operational power envelope of **< 100 μW** .

Ad-Hoc Network Synchronization: Spectral Graph Partitioning

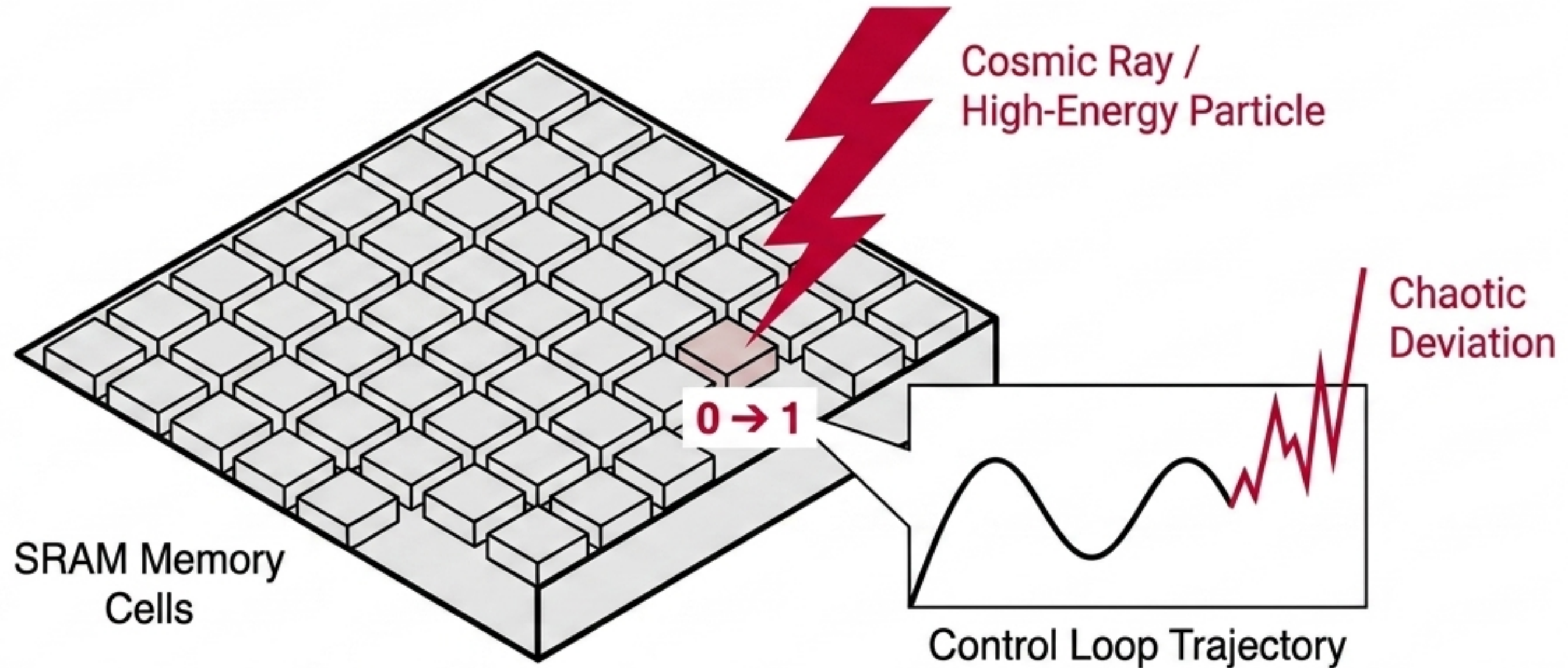


Graph Laplacian: $L = D - A$
(where D is degree matrix, A is adjacency matrix)

Fiedler Vector (λ_2) Calculation
via Deflated Power Iteration

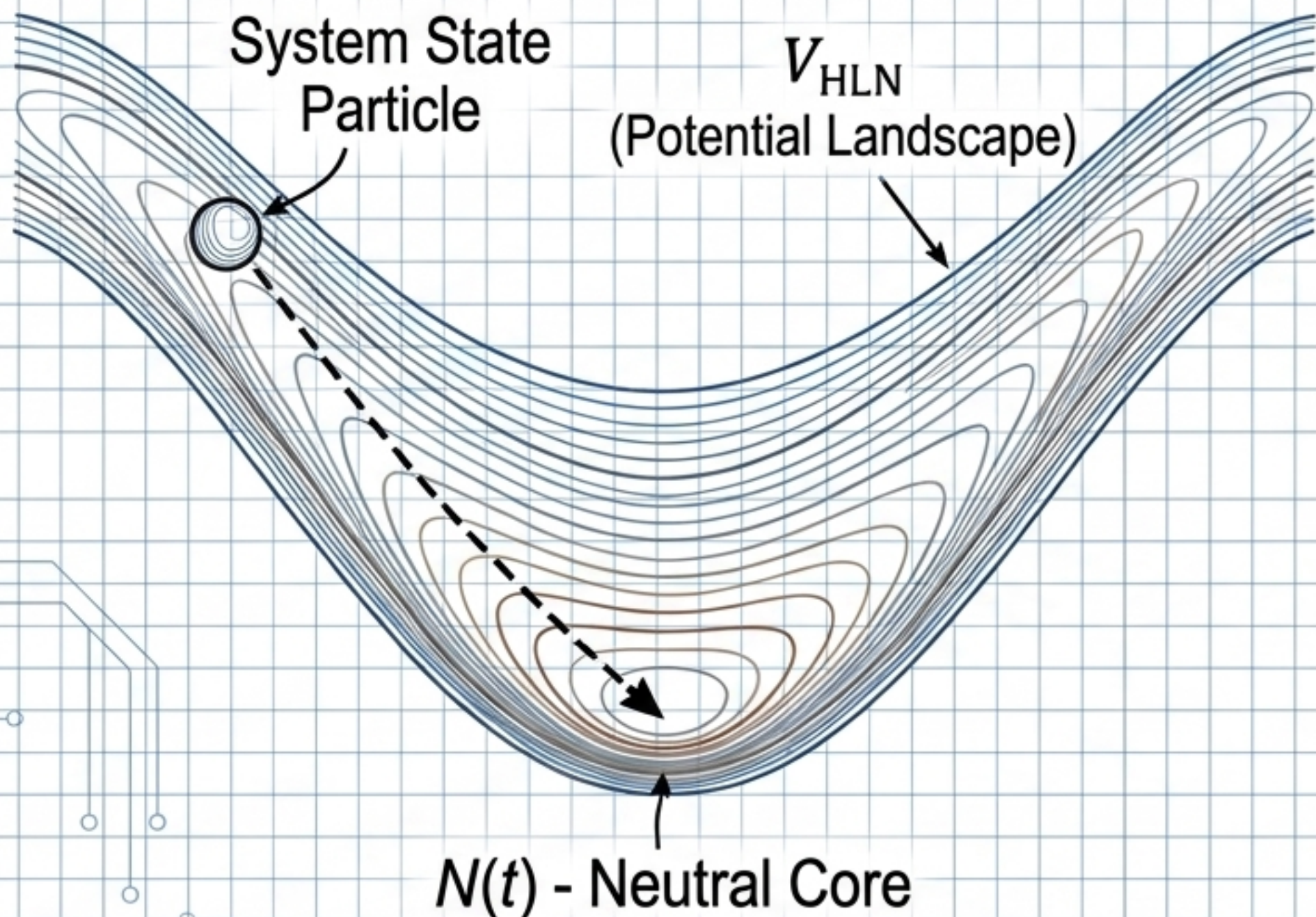
- Local microcontrollers treat the sensor network as an ad-hoc undirected graph.
- Reduces prohibitive $O(N^4)$ complexity to $O(N \cdot M)$ by calculating the Fiedler vector locally at runtime.
- Resolves an 8-node local neighborhood matrix in < 1.15 ms on a 16 MHz core.

The Failsafe Imperative: Surviving Single-Event Upsets (SEUs)



In deep space or high-radiation tactical environments, hardware registers are highly vulnerable to **soft errors**. Standard RTOS architectures **crash** and require **power-cycling** when instruction pointers or heap allocations are corrupted. ALICE is designed for continuous **Bounded-Input Bounded-Output (BIBO) stability**.

High-Low Neutrality (HLN): The Hybrid Safety Net

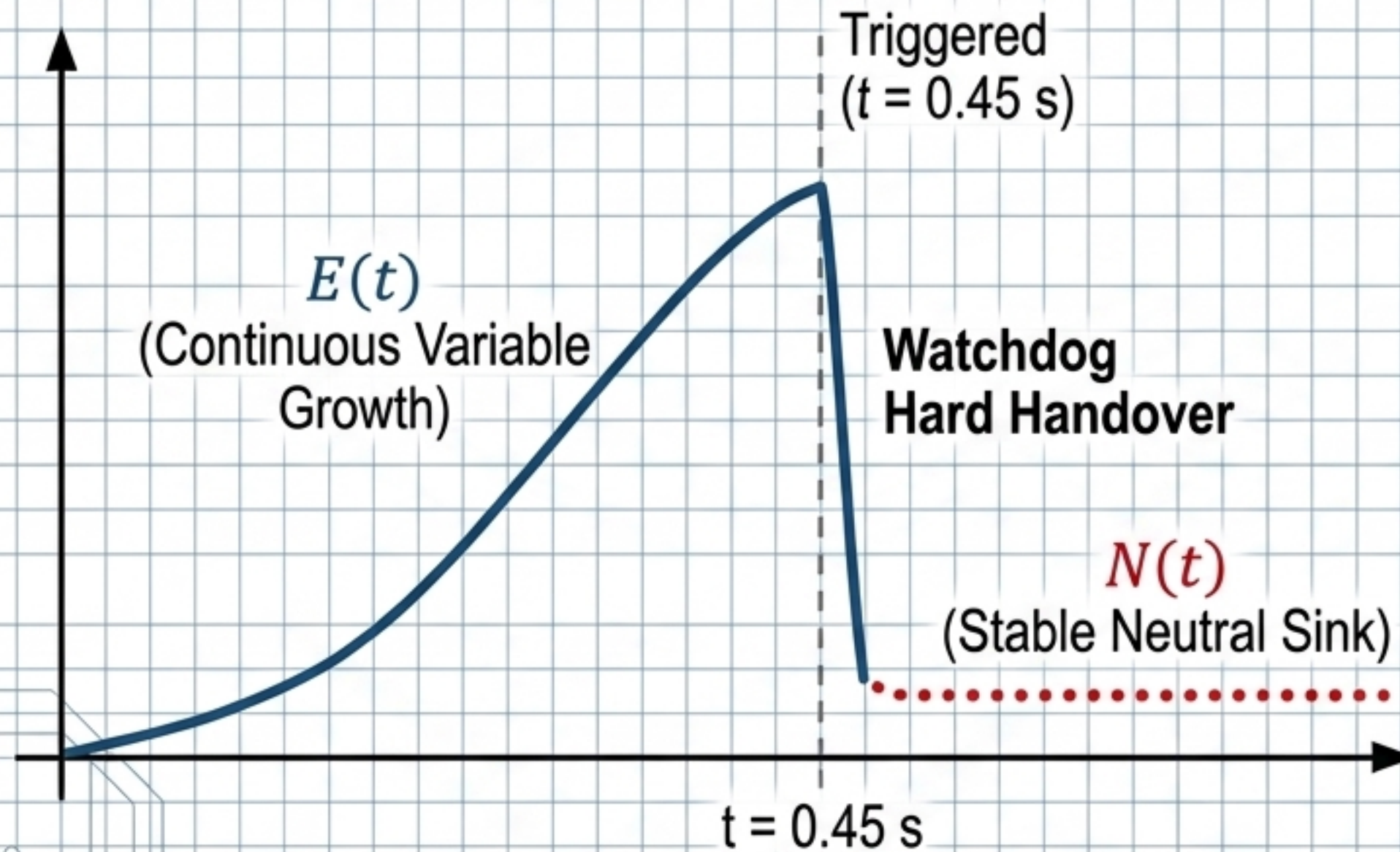


Continuous Attenuation: Operating variables are mapped to an inverted saddle-well. Continuous state changes follow a gradient that provides a natural restoring force, continuously pulling soft errors back toward a stable, neutral core.

Persistence Integral: The system tracks cumulative error over time to detect hard faults:

$$P_E(t) = \int |E(\tau)|^2 d\tau$$

The Watchdog Hard Handover



When the persistence integral exceeds P_{crit} (12.0), the hardware watchdog bypasses the OS.

It executes the **State Reclassification Protocol (SRC)**, dropping variables to zero in a single clock cycle and shifting state to the **Neutral Sink**.

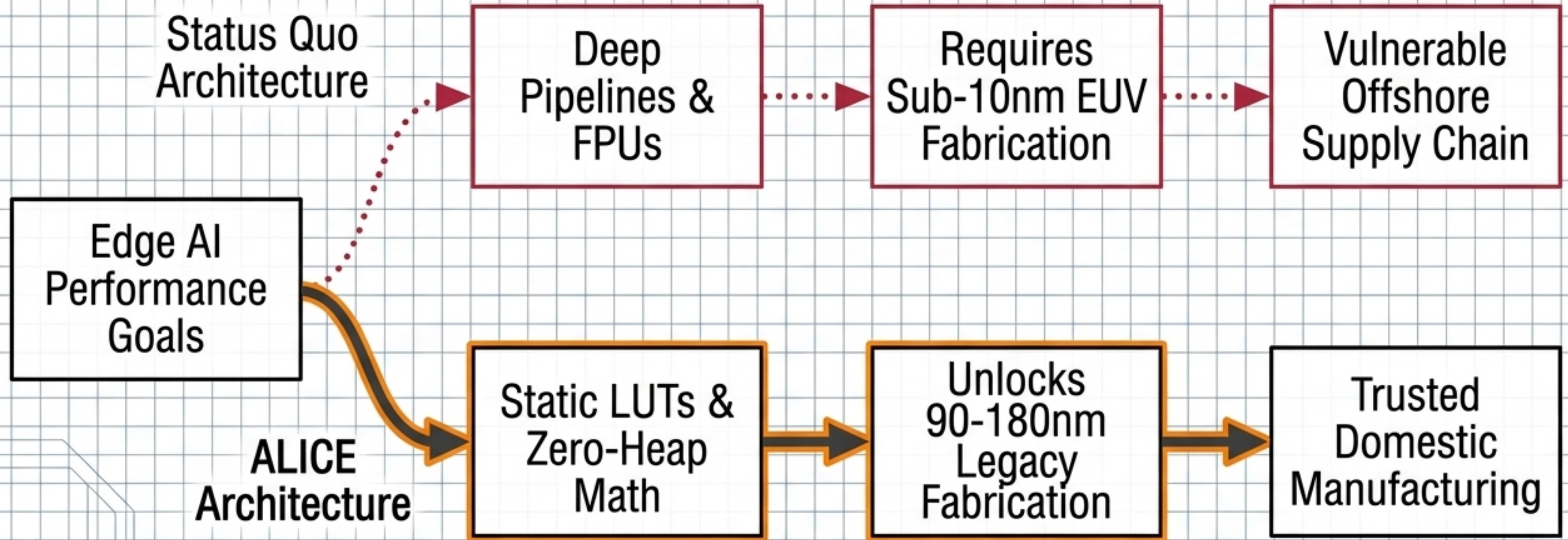
Reviewer Question: How does the discrete handover isolate corrupted SRAM banks without triggering a system-wide reset?

Empirical Proof: Bench Validation Metrics

Table 2: Experimental Verification Summary	
Microcontroller Core	ARM Cortex-M4 (STM32L476RG) @ 16 MHz
Execution Latency	4.2 μ s per fixed-point jump / 18.5 μ s watchdog intervention
Memory Footprint	7.79 KB Flash / 348 Bytes SRAM / 0 Bytes Heap
Fault Robustness Test	10,000 automated injected-fault cycles
Failsafe Recovery Result	99.94% bounded-state retention under hostile conditions

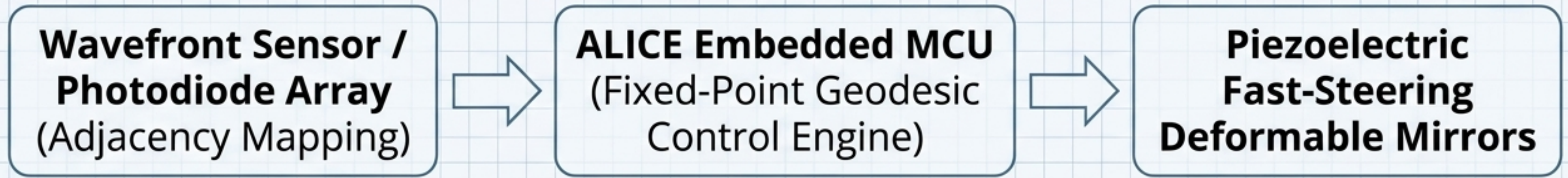
Tested on bare-metal MISRA-C compiled code (-O2). ALICE achieves determinism and μ s latency on commodity 16MHz silicon.

Strategic Positioning: Supply Chain Sovereignty



By decoupling execution efficiency from physical gate dimensions and replacing deep pipelines with static LUTs, ALICE achieves advanced edge AI capabilities entirely on mature, trusted domestic semiconductor manufacturing processes.

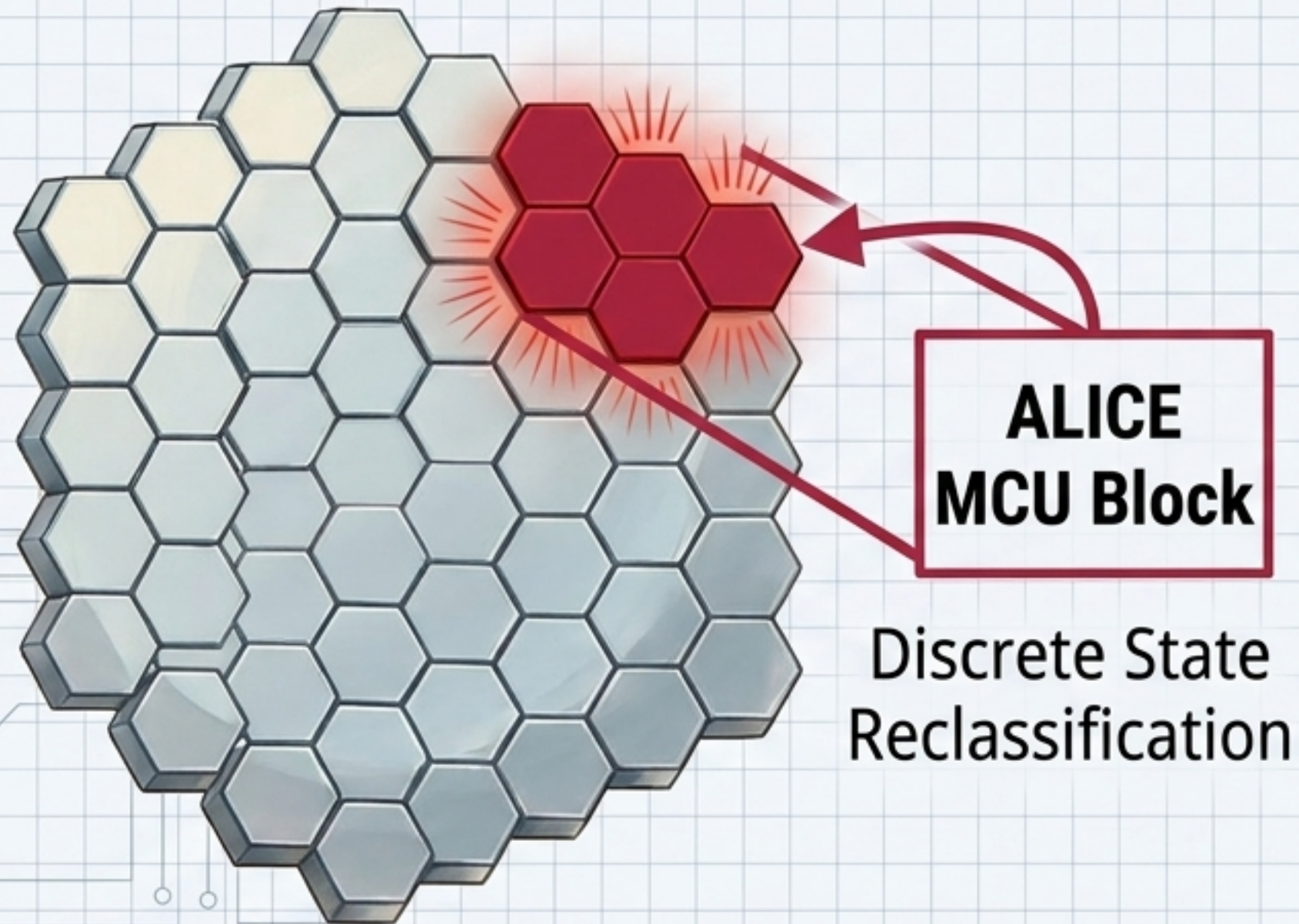
Case Study: SWaP-Constrained High Energy Laser (HEL) Control



Airborne directed-energy platforms suffer from rapid mirror heating and thermal lensing. Traditional adaptive optics require heavy GPUs that violate SWaP constraints.

ALICE provides an ultra-low-SWaP, decentralized control engine to map sensor adjacency directly to physical mirror boundaries without an FPU or RTOS.

Decentralized Actuation & Thermal Blooming Protection



On-Chip Spectral Alignment: MCUs compute the Fiedler vector locally to prioritize actuator adjustments on critical structural boundaries, combating mechanical jitter in real-time.

Catastrophic Optical Damage (COD) Prevention: The HLN watchdog tracks cumulative thermal load per sector. If a sector overheats, ALICE triggers a localized failsafe state to adjust the beam profile without shutting down the entire platform.

Architectural Comparison Matrix

Architectural Feature	Conventional Embedded Runtime	ALICE Resource-Adaptive Runtime
Arithmetic Pipeline	Floating-point (FPU)	Integer-only (Q16.16 Fixed-point)
Memory Allocation	Dynamic (malloc/heap)	Static only (zero heap)
Operating System	RTOS / Embedded Linux	Bare-metal execution
Hardware Core	GPU, FPGA, App Processor	Standard Cortex-M Microcontroller
Power Management	Continuous active polling	Event-driven passive wake-up
Telemetry	Active RF Transmitter (>50mW)	Passive Backscatter (<100μW)
Fabrication Node	Advanced sub-10nm EUV	Domestic Legacy Fabs (90-180nm)

ALICE systematically targets and removes the resource dependencies that cause failure in contested edge environments.

Engineering Honesty: Limitations and Tradeoffs

Optimal ALICE Use-Cases

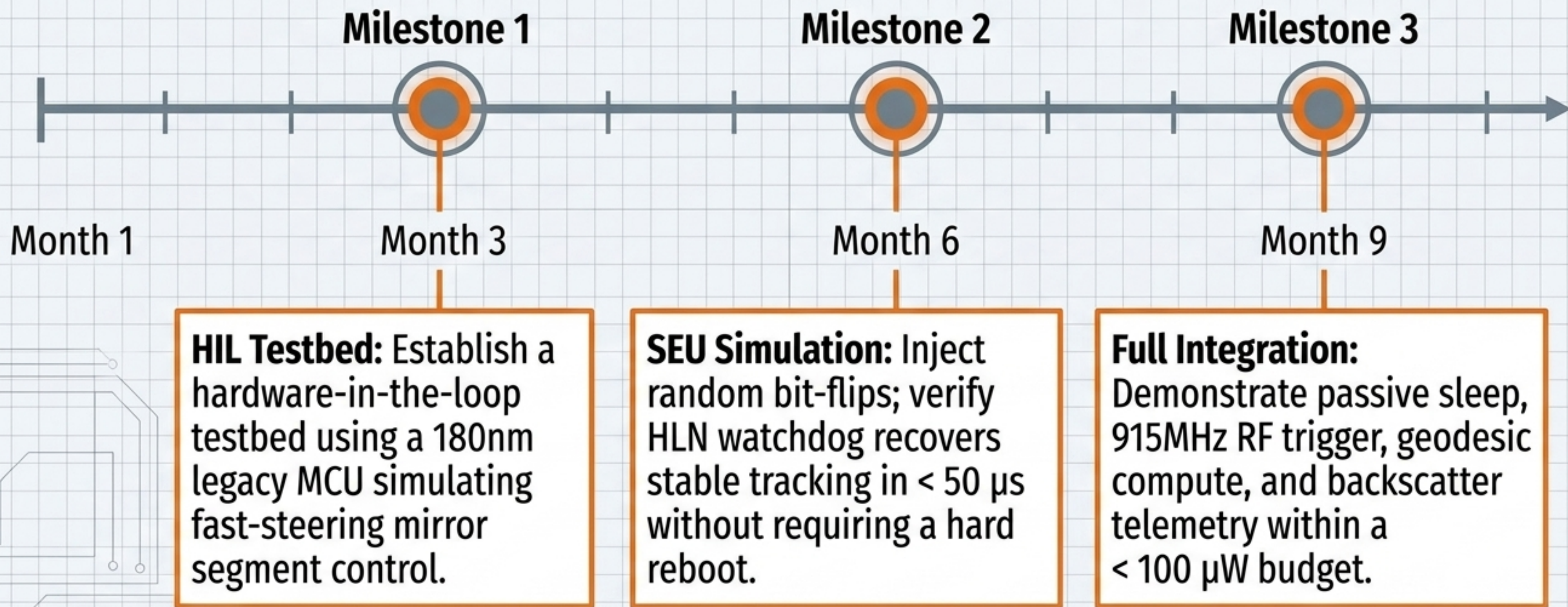
- ✓ Deterministic hardware control
- ✓ Closed-loop sensor synchronization
- ✓ Ad-hoc state tracking in sparse networks
- ✓ Extreme radiation / SEU environments

Out-of-Scope / Sub-Optimal

- ✗ General-purpose computing / OS tasks
- ✗ Heavy string and text processing
- ✗ Unstructured neural net generation at runtime
- ✗ Dynamic payload routing protocols

ALICE is not a general-purpose OS. Shifting complexity offline means runtime flexibility is traded for extreme robustness. It cannot dynamically allocate memory for unpredictable data types or execute non-precompiled generative math at the edge.

Future Work: Phase I Demonstration Workplan (TRL 3 $\rightarrow$ 4)



Securing the Tactical Edge: Key Takeaways

1. Offline-to-Online Geometric Compression

Eliminates the FPU and the Heap.
Reduces numerical solvers to
pre-compiled fixed-point LUTs.

**ALICE
Core**

2. Watchdog-Backed Hardware Resilience

HLN failsafe guarantees bounded-
state retention and 99.94% recovery
from Single-Event Upsets.

3. Supply Chain Sovereignty

Decouples performance from physical gate
dimensions, unlocking execution on trusted
domestic 90-180nm legacy fabs.

By mapping offline quantum information geometry onto legacy hardware, ALICE bypasses von Neumann limitations to achieve continuous operational sovereignty. Ready for Hardware-in-the-Loop demonstration at the August 2026 Hanover Workshop.