Low-Resource Computing: The Resource-Adaptive Embedded Runtime (ALICE)

A Physics-First Architecture for Contested, Austere, and Long-Duration Environments

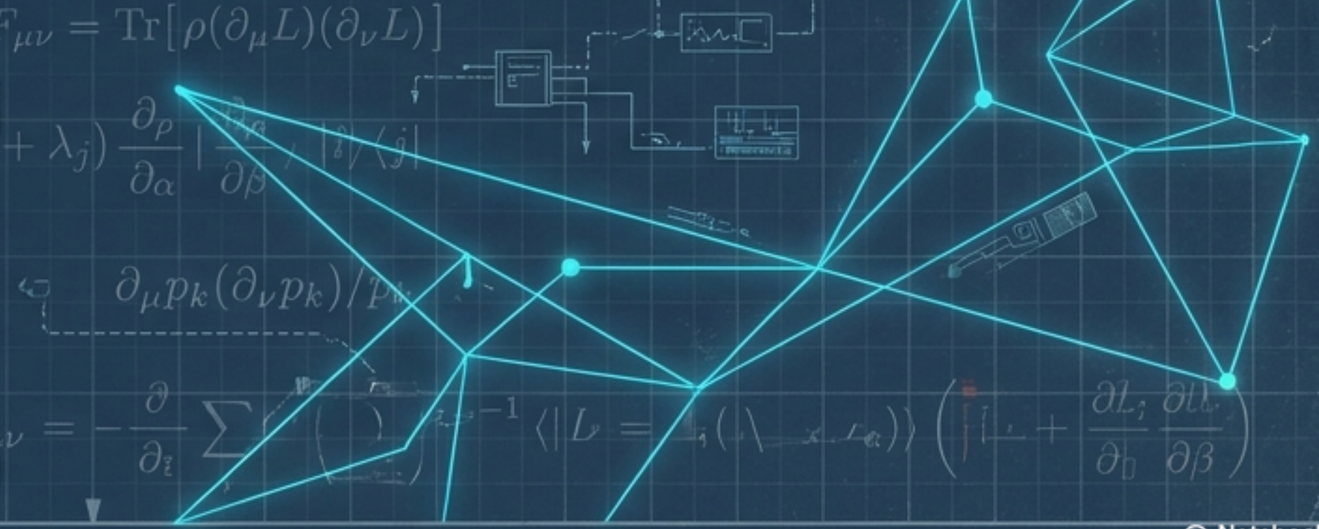
CLASSIFIED - SENSITIVE

Respondent: Niratech Corp

Target Office: DARPA Multi X Office (MXO) / Strategic Technology Office (STO)

Principal Investigator: George Nero Lindstrom Jr.

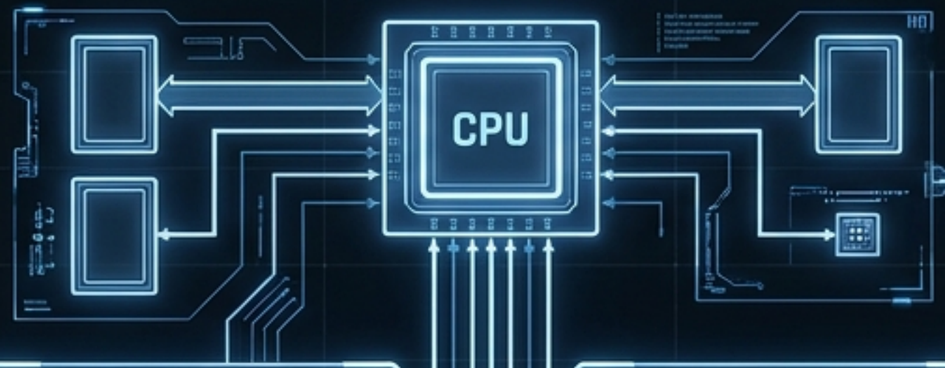
Reference: DARPA-SN-26-82



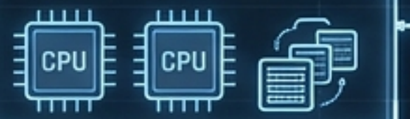
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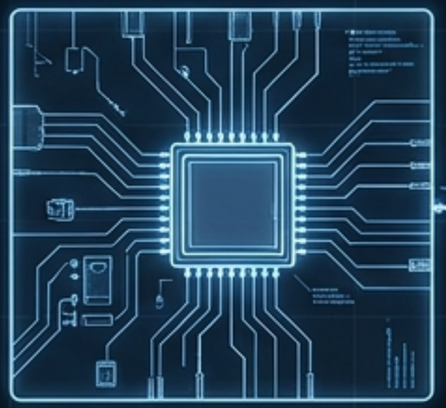
THE AUSTERE COMPUTING CHALLENGE

THE VON NEUMANN ASSUMPTIONS



- ABUNDANT COMPUTATION CAPABILITIES





- STABLE, MACROSCOPIC POWER GRIDS



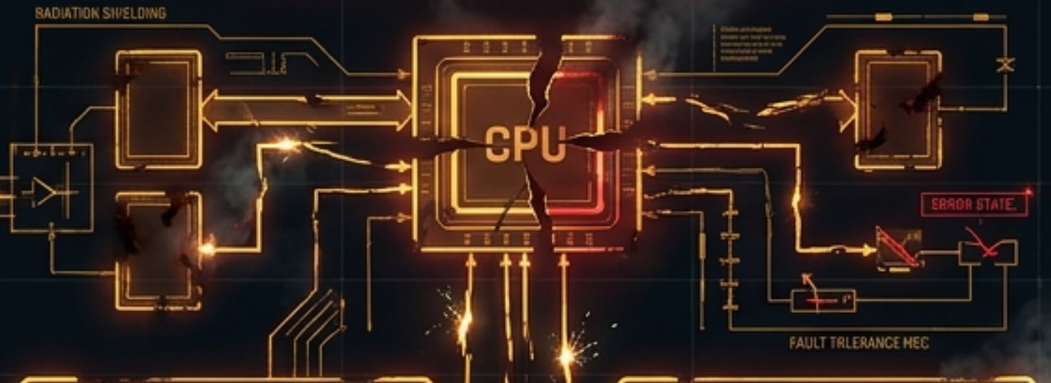
- EXPANSIVE VOLATILE MEMORY (SRAM/DRAM)



- HIGH-BANDWIDTH CONNECTIVITY



THE EXTREME EDGE REALITY



- INTERMITTENT OR COMPLETELY DENIED POWER



- HIGHLY VOLATILE, SINGLE-EVENT-UPSET (SEU) PRONE RADIATION ENVIRONMENTS



- SPORADIC, JAMMED AD-HOC COMMUNICATION



- STRUCTURAL RELIANCE ON LEGACY, COARSE-PROCESS FABRICATION NODES

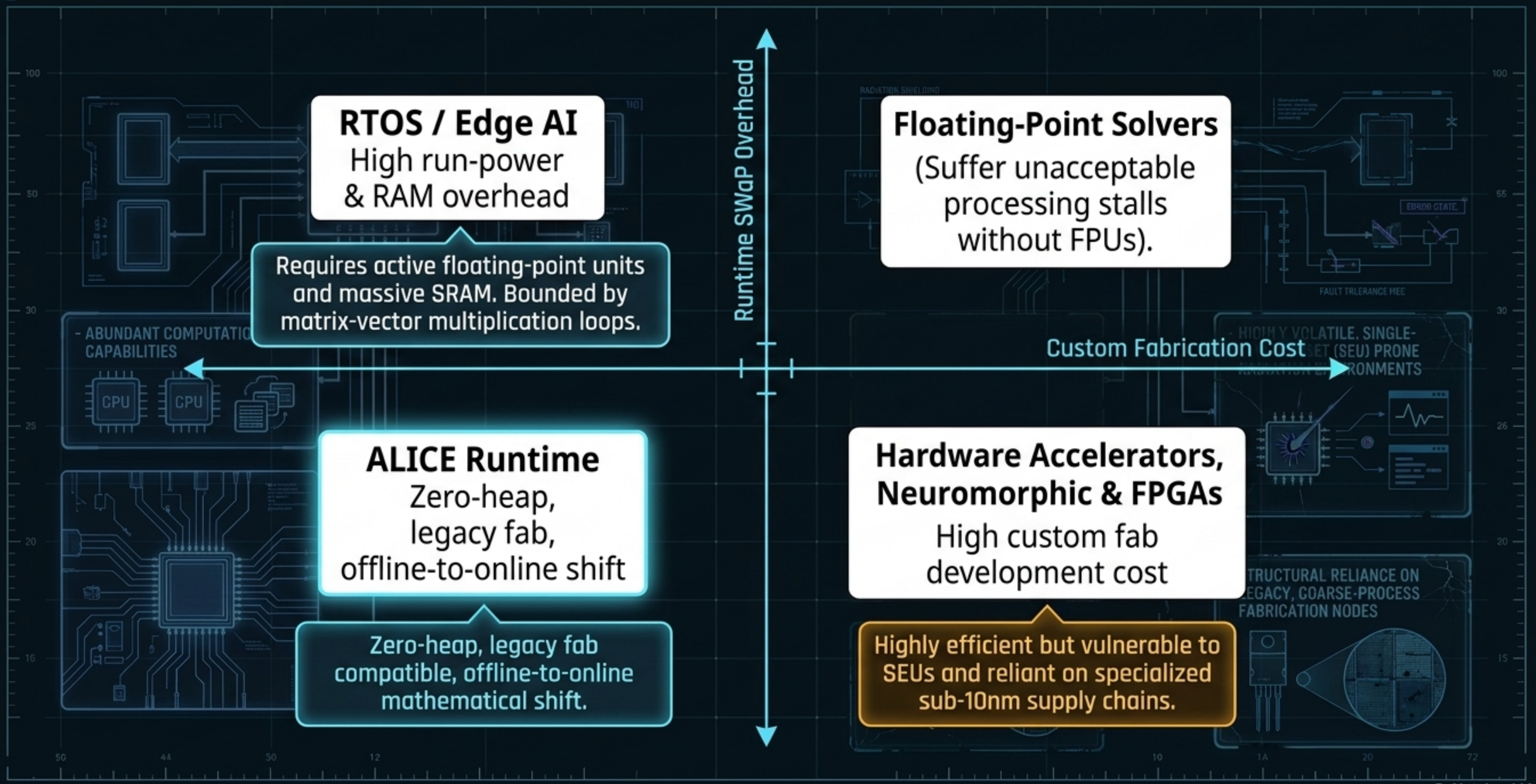


- STRUCTURAL RELIANCE ON COMMUNIICATION



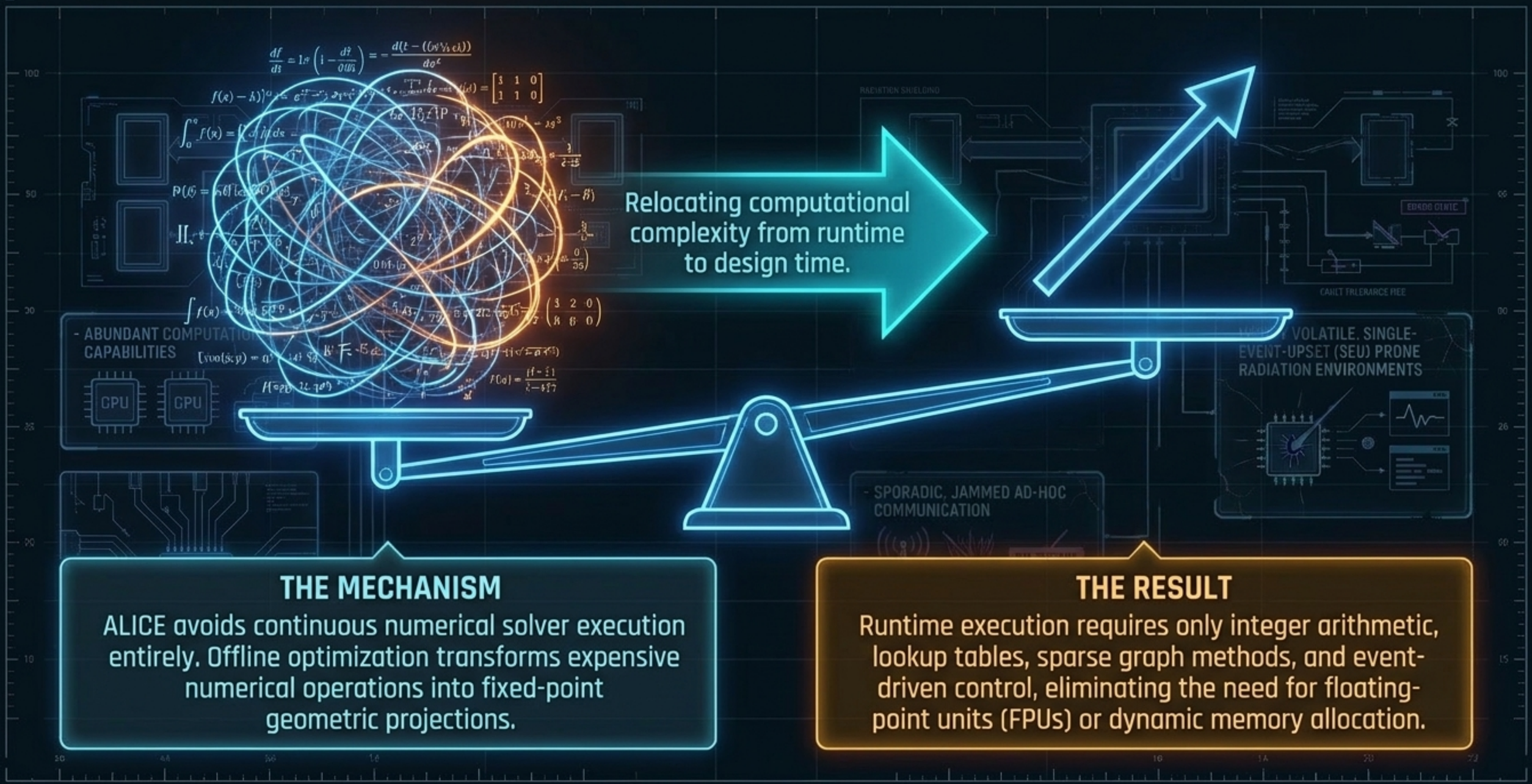
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THE PARADIGM SPECTRUM: POSITIONING THE ALICE EXECUTION PROFILE



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THE CENTRAL TECHNICAL HYPOTHESIS



THE MECHANISM

ALICE avoids continuous numerical solver execution entirely. Offline optimization transforms expensive numerical operations into fixed-point geometric projections.

THE RESULT

Runtime execution requires only integer arithmetic, lookup tables, sparse graph methods, and event-driven control, eliminating the need for floating-point units (FPUs) or dynamic memory allocation.

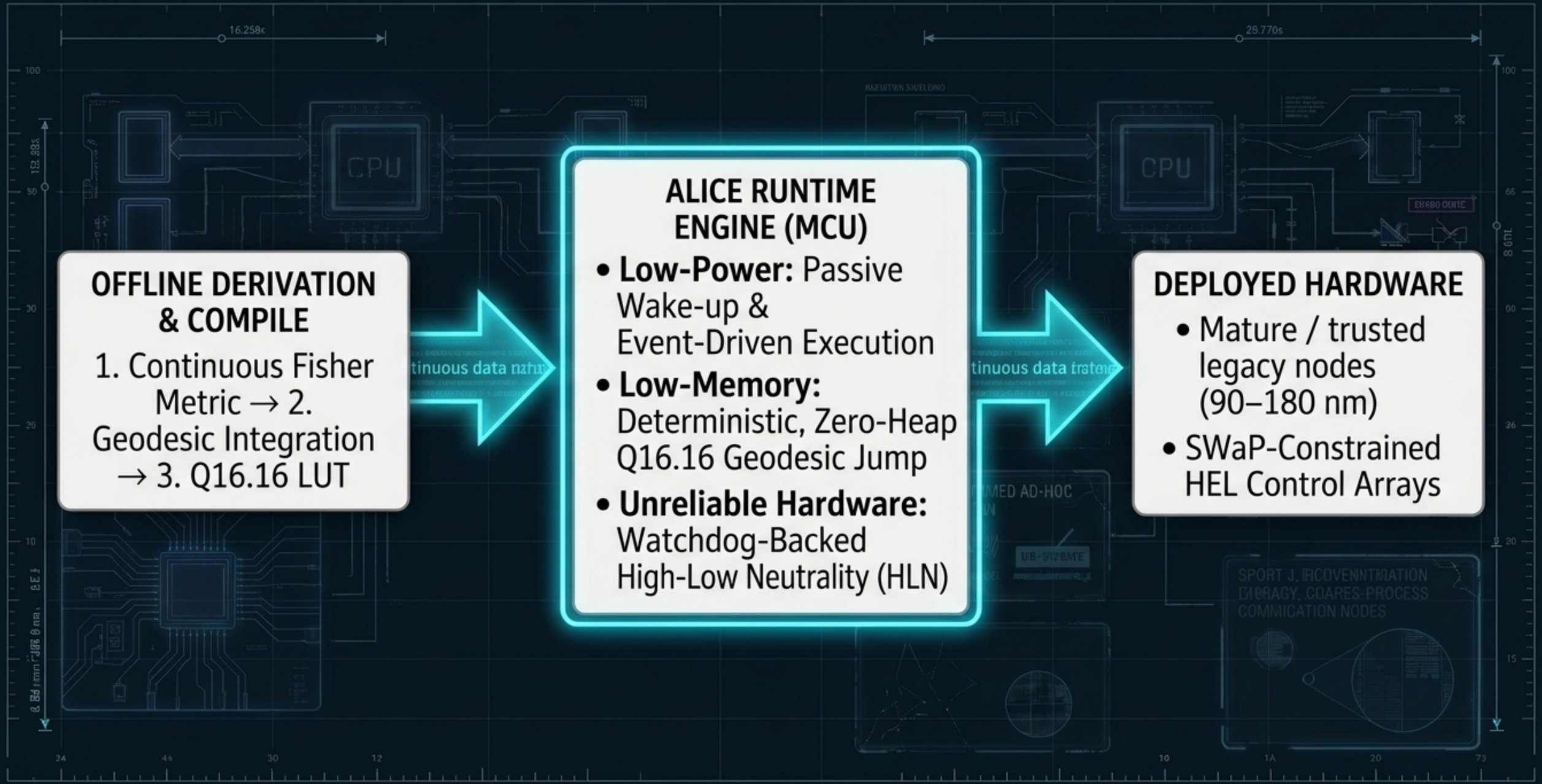
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ARCHITECTURAL DIAGNOSTIC MATRIX

FEATURE	CONVENTIONAL EMBEDDED RUNTIME	ALICE RUNTIME
Arithmetic Pipeline	Floating-point (FPU required)	Integer-only (Q16.16 Fixed-point)
Memory Allocation	Dynamic (malloc/heap-dependent)	Static only (malloc is strictly forbidden)
Operating System	RTOS / Embedded Linux	Bare-metal execution
Hardware Core	GPU/FPGA/App Processor	Standard low-cost Microcontroller (Cortex-M)
Power Management	Continuous active polling	Event-driven passive wake-up
Telemetry Radio	Active RF transmitter (>50 mW)	Passive backscatter modulator (<100 µW)
Fabrication Node	Advanced sub-10 nm CMOS	Mature, domestic legacy nodes (90–180 nm)

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End-to-End Operational Flow



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Pillar 1: Event-Driven Passive Wake-up & Telemetry



915 MHz Antenna

Impedance Matching Network

Schottky Diode Detector Array

Acts as a non-linear square-law detector rectifying high-frequency AC into a DC envelope.

TLV3691 Ultra-Low Power Comparator

Draws just 75 nA. Trips when voltage > 50 mV.

Microcontroller GPIO State Driver

Awakens the core via EXTI0 interrupt.

Key Takeaway (Backscatter): Telemetry is transmitted via passive backscatter modulation (toggling an ADG901 RF switch), avoiding power-hungry active RF synthesizers. Total power envelope: <100 µW.

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Pillar 2: Open Quantum Systems & Ambient Resonance

The Physical Bridge

Transducing a macroscopic classical RF drive into a measurable voltage by modeling the substrate as two-level systems interacting with an ambient electromagnetic field.

$$\frac{d\rho}{dt} = -i\frac{i}{\hbar}[H_0 + H_I(t), \rho] + \sum_j \gamma_j \left(L_j \rho L_j^\dagger - \frac{1}{2}\{L_j^\dagger L_j, \rho\} \right)$$

The Analog Result

The rectified output voltage is a direct, classical measurement of the down-converted quantum state trace operation:

$$V_{\text{out}}(t) = \kappa \cdot g(t)^2 \cdot |\text{Tr}(d\rho(t))|^2$$

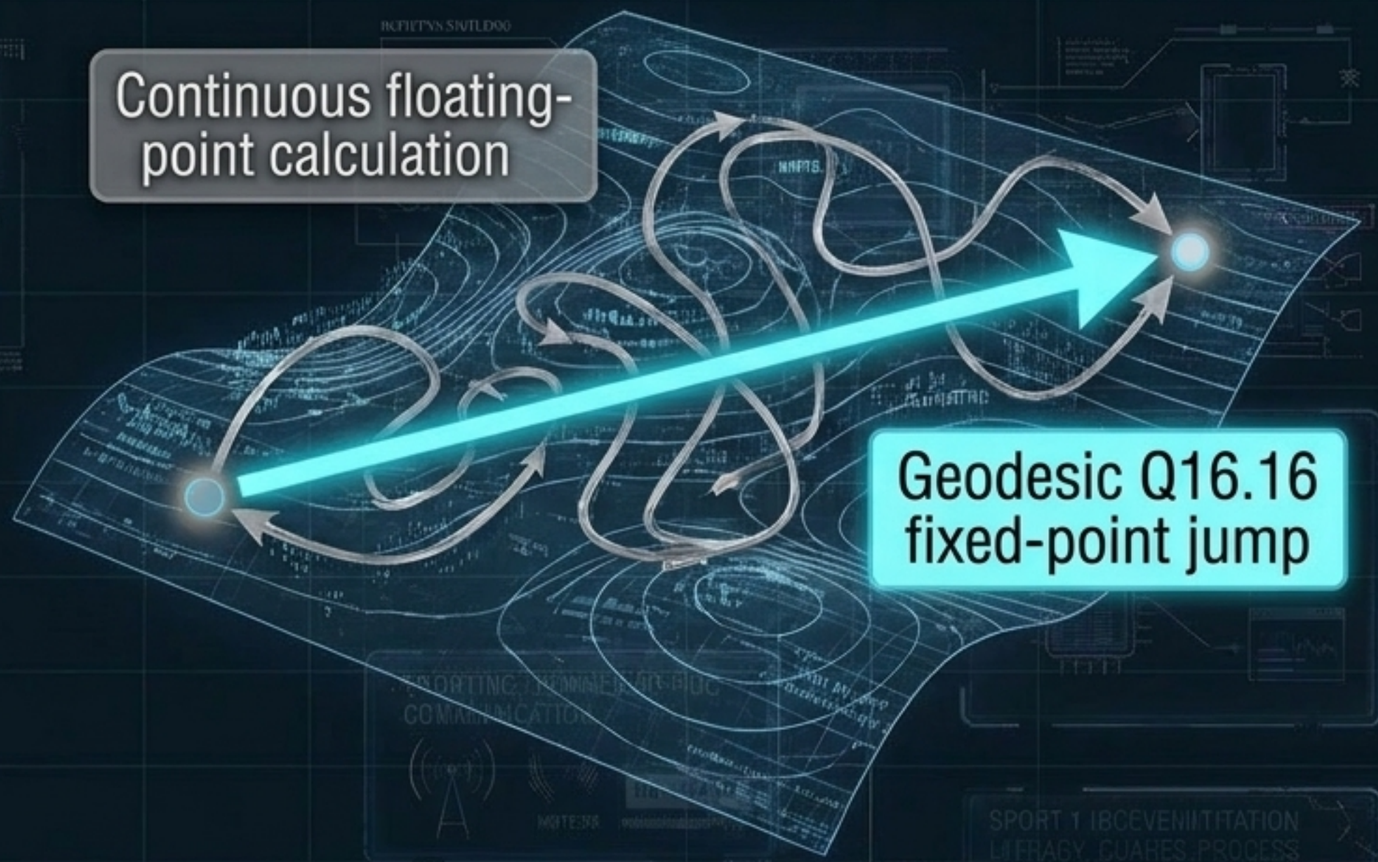
Decoherence-Free Subspace

Logical qubits mapped to entangled singlet configurations protect the state from common-mode thermal dephasing.

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Pillar 3: Information-Geometric Compression

1. **Map:** System states are mapped as coordinates on a continuous manifold governed by the Quantum Fisher Information Metric (QFIM).
2. **Integrate:** Christoffel symbols are computed offline to integrate representative geodesic trajectories.
3. **Quantize:** Displacement vectors are quantized into fixed-point lookup entries.



The Insight: ALICE does not execute information geometry symbolically at runtime. It executes a pre-calculated fixed-point projection derived offline.

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Deterministic Q16.16 Fixed-Point Execution

```c
typedef int32_t fixed32_t;
#define Q_FRAC_BITS   16
#define Q_HALF        ((fixed32_t)(1 << (Q_FRAC_BITS - 1)))

static inline fixed32_t q_mul(fixed32_t a, fixed32_t b) {
    int64_t temp = (int64_t)a * (int64_t)b;
    return (fixed32_t)( (temp + Q_HALF) >> Q_FRAC_BITS);
}
```

Zero Heap: malloc is strictly forbidden.

Execution Speed: Reduces a complex differential equation network into a single multiplication/addition sequence. Compute latency is just 4.2 µs.

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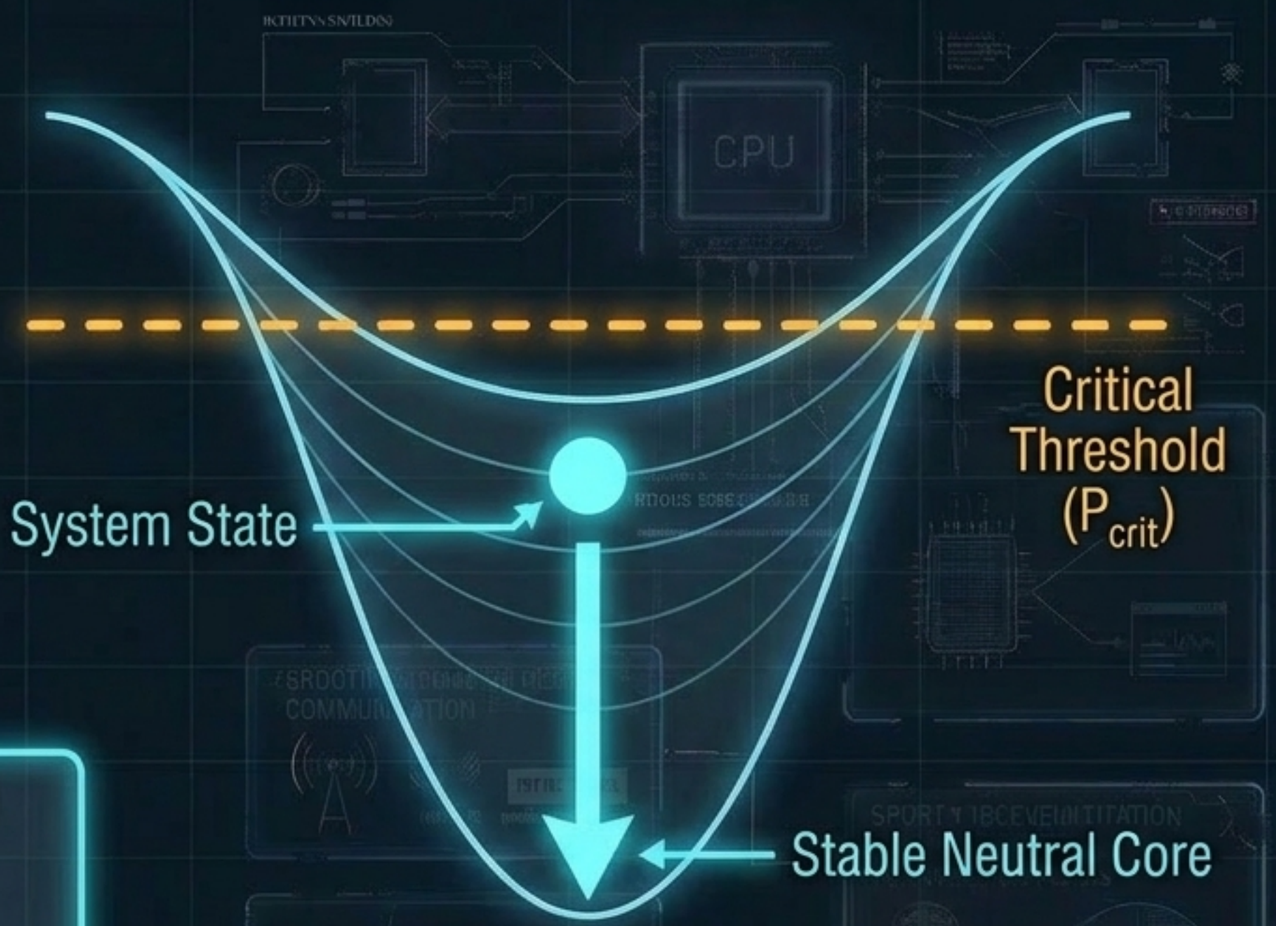
Pillar 4: Watchdog-Backed High-Low Neutrality (HLN)

The Threat: In high-radiation fields, registers are vulnerable to Single-Event Upsets (SEUs) and soft errors.

Continuous Attenuation: Operating variables follow a gradient that provides a natural restoring force, pulling soft errors back toward the neutral core:

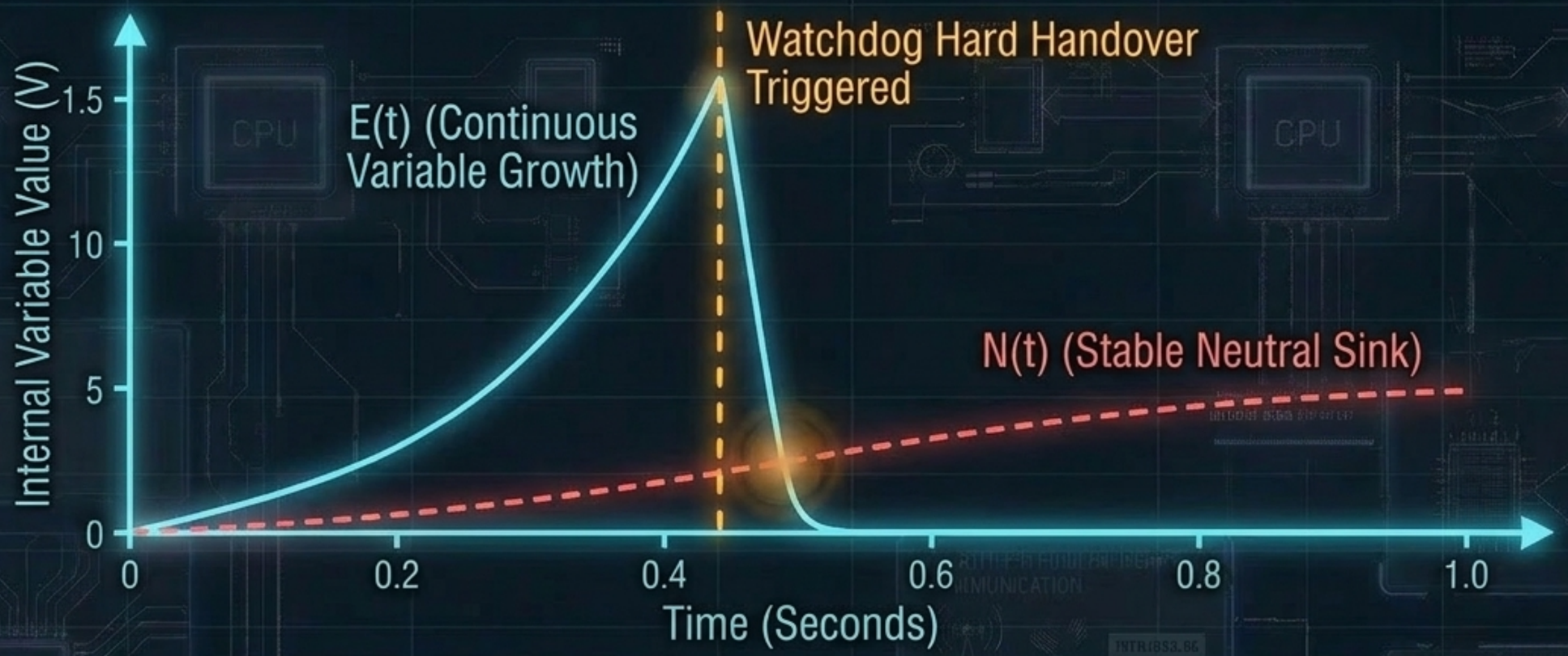
$$V_{HLN}(E,P,N) = k_n N - k_e |E| - k_p |P|$$

Discrete Watchdog: If the persistence integral exceeds P_{crit}, the hardware watchdog triggers a State Reclassification Protocol. Memory registers are cleared and threads restart instantly without a system-wide reboot.



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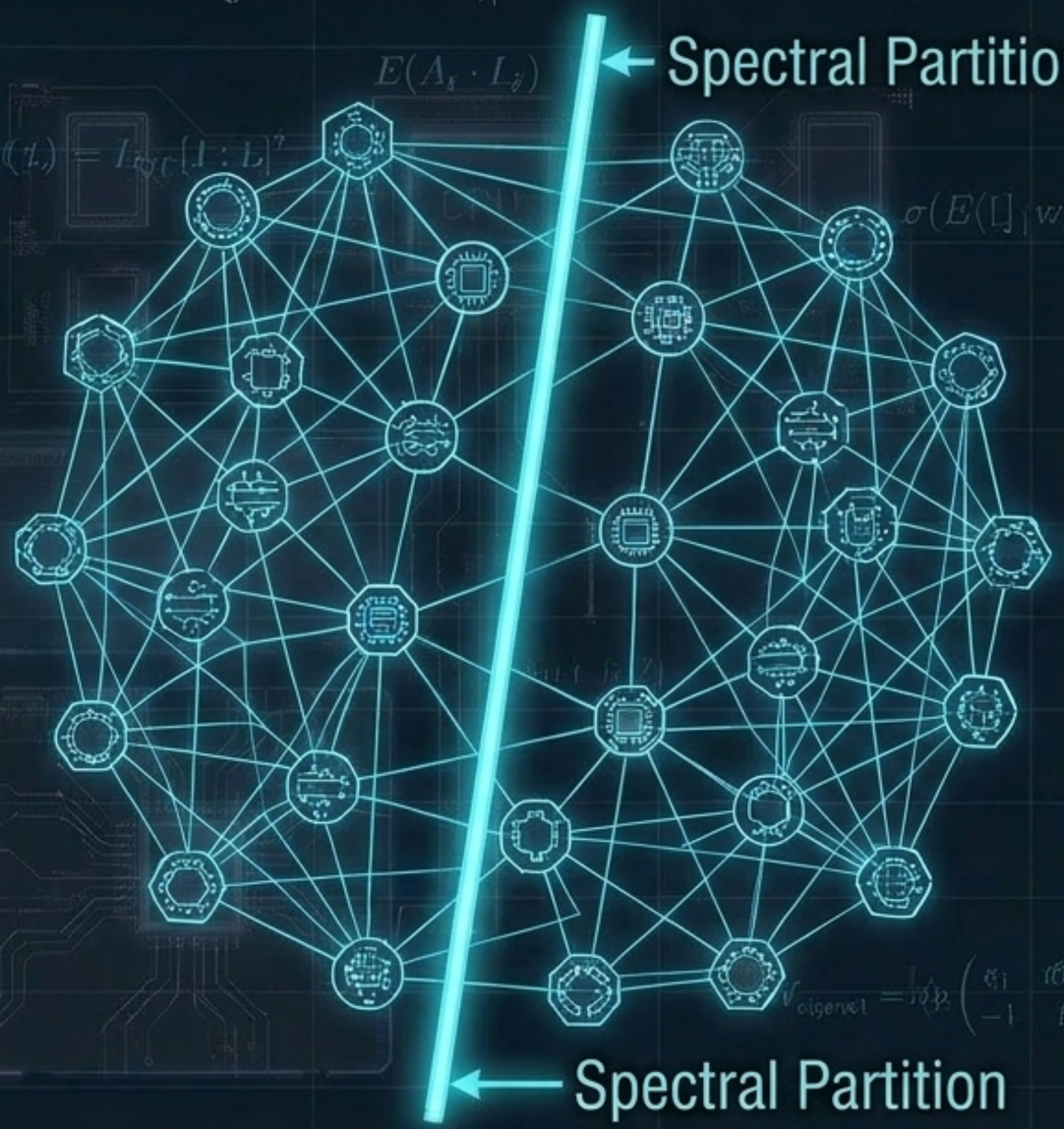
Fault Recovery: Bounded-State Retention Under Injected SEUs



The Result: Under artificially injected control instability (environmental noise outpacing physical damping), the continuous variables were suppressed to 0.0 V in a single clock cycle. Maintained 99.94% bounded-state retention across 10,000 automated fault injection cycles.

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Pillar 5: Spectral Graph Partitioning & Ad-Hoc Synchronization



The Concept: Distributed nodes coordinate without a central server by treating the network topology as an undirected graph.

The Algorithm: Using a deflated power iteration algorithm, nodes calculate the Fiedler vector (the eigenvector of the second-smallest eigenvalue of the Graph Laplacian) in real-time.

Performance: Reduces O(N^4) complexity to O(N · M). Resolves an 8-node local neighborhood matrix in under 1.15 ms on a 16 MHz microcontroller.

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Synthesis: Decoupling Performance from Silicon Scaling



Traditional edge computing achieves performance gains through advanced sub-10nm fabrication nodes—a fragile, overseas supply chain.



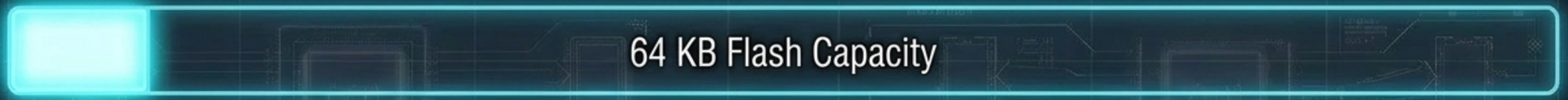
By replacing deep pipelines and branch predictors with static geodesic lookup tables, ALICE enables complex, non-linear AI and adaptive control on cheap, trusted, and domestically sourced 90-180 nm legacy nodes.

Complexity is solved by structure, not by silicon limits.

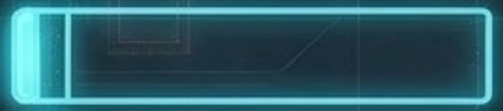
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Empirical Profiling: The 7.79 KB Control Stack

Memory Map



Total ALICE Stack: 7.79 KB Flash



Total Dynamic Heap: 0 Bytes | Static: 348 Bytes

Fixed-Point Core Math:
1.12 KB Flash | <1.0 µs latency

Geodesic LUT: 3.45 KB Flash
12 Bytes SRAM | 4.2 µs latency

Spectral Partitioner: 2.38 KB Flash
312 Bytes SRAM | 1.15 ms latency

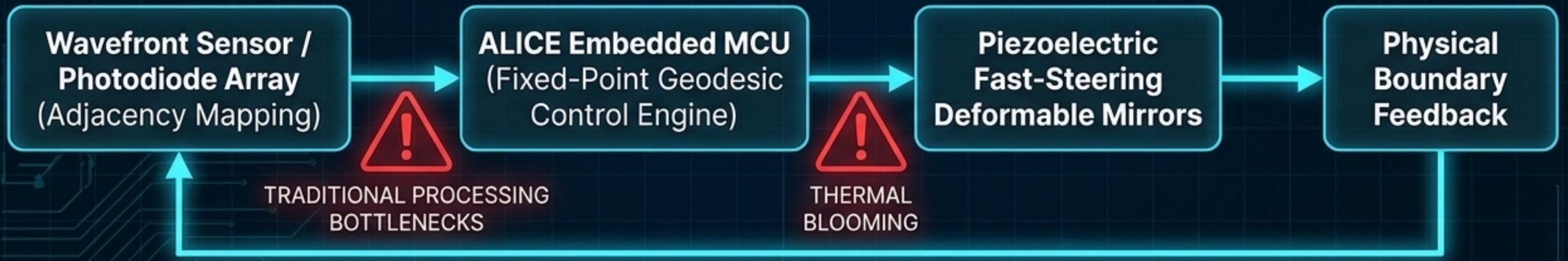
HLN Failsafe Engine: 0.84 KB Flash
24 Bytes SRAM | 18.5 µs latency

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Strategic Application: SWaP-Constrained High Energy Lasers

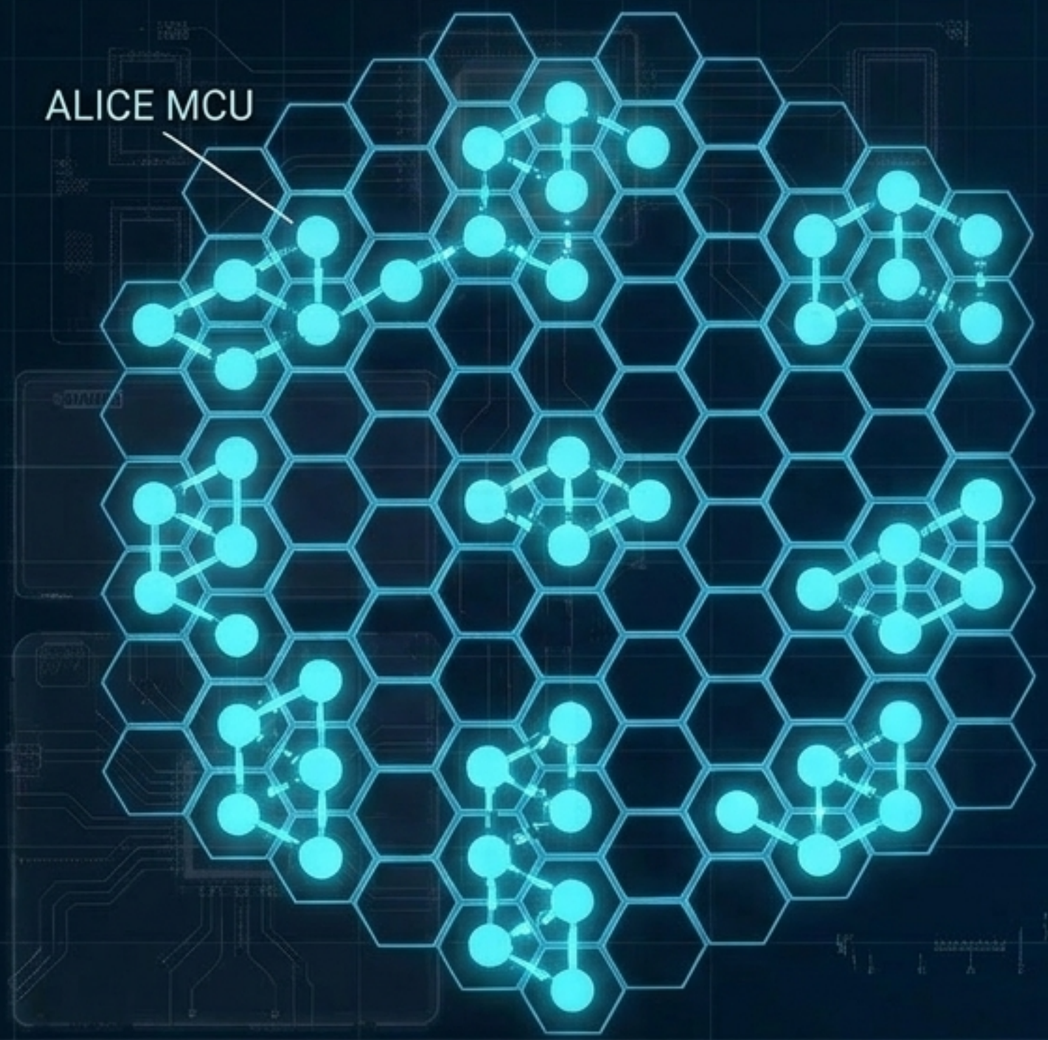
The Problem: HELs on mobile/airborne platforms suffer from rapid mirror heating, mechanical jitter, and localized thermal lensing.

The Bottleneck: Standard adaptive optics require power-hungry GPUs or FPGAs to run real-time wavefront reconstruction, violating the strict **Size, Weight, and Power (SWaP)** constraints outlined in **DARPA-SN-26-82**.



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The Decentralized ALICE HEL Architecture



Decentralized Control: Mirror partitioned into localized segment clusters, each controlled by a localized segment clusters, each controlled by a dedicated legacy micro-controller running ALICE.

On-Chip Spectral Alignment: Nodes treat actuator-sensor coupling as an ad-hoc graph, prioritizing adjustments on critical structural boundaries to compensate for jitter without a central server.

Fault-Tolerant Protection: The HLN watchdog tracks cumulative thermal load on individual segments. If a sector overheats, it triggers discrete state reclassification to adjust the beam or actuate cooling, preventing Catastrophic Optical Damage (COD) without shutting down the laser.

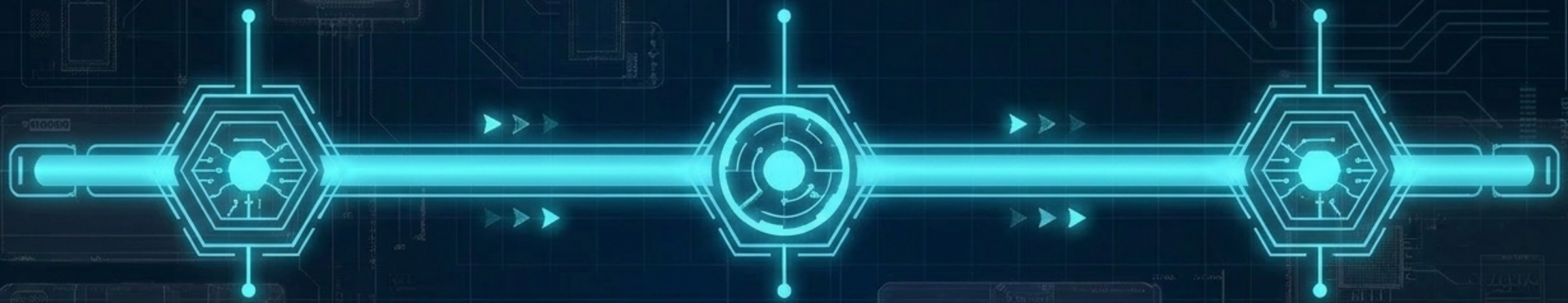
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Phase I Demonstration Workplan (TRL 4)

Months 1–3

Milestone 1: Hardware Integration & Baseline Testing. Establish a Hardware-in-the-Loop (HIL) testbed using a 180nm legacy legacy microcontroller controlling a simulated fast-steering mirror.

Months 4–6



Milestone 2: SEU Simulation. Inject random bit-flips into system registers to verify the HLN watchdog recovers stable tracking in <50 µs without a hard reboot.

Months 7–9

Milestone 3: Full HIL Demonstration. Execute an event-driven tracking loop: passive sleep -> 915 MHz RF RF wake-up -> geodesic optimal control computation -> passive backscatter telemetry. Total power envelope: <100 µW.

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Execution Readiness: August 2026 Workshop



ALICE represents a proven transition from abstract mathematical physics to deterministic, field-ready hardware execution. Complexity is solved by structure, ensuring operational sovereignty at the extreme edge.

Physical microcontroller test hardware, bench-validation results, and real-time HIL simulations will be presented at the Low Resource Computing Workshop in Hanover, New Hampshire.

Niratech Corp // CAGE: 11F83 // UEI: MP6QBYRXTS75

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